REMARKS

Claims 1-11 and 15-18 are in the case. The claims are objected to. Claims 9-11 and 15-18 are allowed, for which the applicants thank the examiner. Claims 1-8 are rejected under 35 USC § 103 over USPN 6,707,936 to Winter et al. in view of USPN 5,475,695 to Caywood et al. Claims 1-3, 6-11, and 15-17 are hereby amended to overcome the objections. The rejections are respectfully traversed. No new matter has been introduced by the amendments, which are supported by the disclosure of the original claims and the specification. These amendments are not made so as to overcome any prior art cited by the examiner. Rather, these amendments are made to ensure that there is no misunderstanding of the language used in the claims, and to correct what the examiner saw as antecedent basis problems in the claims. Thus, there is no narrowing or loss of equivalents in the claims by operation of these amendments.

PRELIMINARY COMMENTS ON REJECTIONS

Three different kinds of information are described between the present claims and the cited references, which are (1) design information, (2) defect information, and (3) failure information. Design information is used as the pattern to construct the integrated circuit. Defect information is generated by performing an "inspection" of the substrate on which the integrated circuits are formed. "Defects" are physical anomalies that can be "seen," such as by an optical method or an electron microscope, for example. Test information, on the other hand, is not detected with an inspection, rather it is determined by "testing" the operation of the integrated circuit, or relevant portion thereof, with an electrical test.

Thus, there is a difference between "defects" and "failures," and between "inspection" and "testing." Stated another way, "defects" are physical anomalies and "failures" are electrical anomalies; "inspection" looks for the physical anomalies and "testing" looks for the electrical anomalies. The present invention as claimed is directed toward correlating design data with defect data.

CLAIM REJECTIONS UNDER §103

Independent claim 1 claims, *inter alia*, a method for producing yield enhancement data by comparing a database of physical defects to a database of design information, and associating the physical defects with classes of design information by location on the substrate of both the physical defects and elements of the design information.

The combination of Winter et al. and Caywood et al. does not describe such a method. Applicants first compare the primary reference against the elements of the claim as recited above, to determine wherein the primary reference is deficient. Then the secondary reference is analyzed to determine whether it compensates for the deficiencies detected in the primary reference. If both of the references are deficient as to the same element or combination of elements, then the claim is patentable over the cited references.

As described in the abstract and made clear in figure 5, Winter et al. describe using design information 18 to generate failure information 21. Actual defects 25 are then found on a wafer. The failure information 21 is applied to each defect 25 to yield a probability value. All the probability values are combined to predict a survival probability for a device on the wafer, and for the wafer itself. Without being bound to not argue otherwise, applicants will accept for the present discussion that the survival probability is yield enhancement data. Thus, it could be said that Winter et al. apply ***theoretical failure information*** to ***defect information*** to obtain ***yield enhancement data***.

However, even with the concessions as made above, the disclosure of Winter et al. falls short of the present invention as claimed in some important aspects. First, Winter et al. do not associate the ***design information*** itself with the defects. Instead, Winter et al. apply the ***theoretical failure information*** to the defects. Although the failure information is generated from design information, this intermediate step makes the present invention as claimed patentably different from Winter et al., because different things are being associated. Second, Winter et al. do not describe associating defects with ***classes*** of design information, or even ***classes*** of the theoretical failure information. Winter et al. do not describe putting that type of information into classes at all. Thus, there are at least two important deficiencies in regard to Winter et al.

We next inspect Caywood et al. to determine whether they remedy the two deficiencies of Winter et al. Caywood et al. do not remedy the deficiencies of Winter et al., in that Caywood et al. also do not describe associating classes of design information with defects. Caywood et al. describe using design information to identify electrical faults ***that can be caused by defects***. That's a theoretical process. The circuit design is analyzed to determine what the response from the faults would be to various input patterns. These tests are then applied to an actual device under test, and the response from the device under test is used to determine the nature of any actual defect that causes the device to fail. This information can then be used to change the manufacturing process.

Thus, Caywood et al. describe finding defects with tests that have been constructed from design information. The design information indicates what tests will identify different kinds of defects, the tests are performed, and the defects are identified. The process is then changed so as to not produce those kinds of defects, if they are found.

By contrast, the present invention as claimed uses location information as a pointer into the design information to determine a class of structure located in that given location, and uses location information as a pointer to the defects to associate the class of structure in the design information with the defect at a given location. Caywood et al. doesn't describe that process at all.

Thus, Winter et al. and Caywood et al. suffer from the same deficiencies, in that neither associates defects with classes of design information by location. Claim 1 patentably defines over the combination of Winter et al. and Caywood et al. Reconsideration and allowance of claim 1 are respectfully requested. Claims 2-8 depend from claim 1 and recite additional important aspects of the invention. For example, claim 8 recites revising the ***design information*** based on the yield information, whereas Caywood et al. describe modifying the ***process*** based on yield information. Therefore, claims 2-8 patentably define over the combination of Winter et al. and Caywood et al. Reconsideration and allowance of claims 2-8 are respectfully requested.

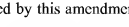
CONCLUSION

Applicants assert that the claims of the present application patentably define over the prior art made of record and not relied upon for the same reasons as given above. Applicants respectfully submit that a full and complete response to the office action is provided herein, and that the application is now fully in condition for allowance. Action in accordance therewith is respectfully requested.

In the event this response is not timely filed, applicants hereby petition for the appropriate extension of time and request that the fee for the extension be charged to deposit account 12-2355. If other fees are required by this amendment, such as fees for additional claims, such fees may be charged to deposit account 12-2252.

Sincerely,

LUEDEKA, NEELY & GRAHAM, P.C.

By: 

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